PDF pour 13666

Le présent fichier PDF présente et fournit des extraits du catalogue :

Flash Memory

1996/1997 Fujitsu semiconductor Data Book

Edité sous le nom Fujitsu
par FALS (Fujitsu AMD Semiconductor Limited) en 1996

Ce catalogue est disponible sous le numéro **AC 13666** dans l'inventaire de la collection de l'ACONIT, Association pour un conservatoire de l'informatique et de la télématique, Grenoble.

Le présent catalogue correspond à une période de maturité dans l'industrialisation et la commercialisation des mémoires flash. Il sera un précieux indicateur des améliorations apportés à ces mémoires flash si on le compare au catalogue édité en 1990 par la société AMD (un catalogue que notre lecteur pourra consulter avec profit - voir collection Aconit n° AC 13371).

Le présent catalogue et un gros livre de 697 pages qui traite des circuits électroniques intégrés constituant les « mémoires flash », et pour cela il fournit :

- une information (1 page) sur la création de FASL, une joint venture entre AMD et Fujitsu ;
- une synthèse (5 pages) des produits offerts en mémoires flash ;
- au chapitre-2 (14 pages), une présentation de la technologie de ces mémoires et particulièrement les améliorations en fiabilité qui ont été réalisées avec : le nouveau montage en Negative Gate Erase Technology (NOR structure) ; Les améliorations réalisées dans les algorithmes embarqués ;
- au chapitre-3 (14 pages), encore pour améliorer la fiabilité, une présentation du plan de qualité, avec en particulier : le SPC (Statistical Process Control présenté en page 38) ; le programme des Investigations and Proposal for Actions to Prevent Recurrence (page 41) ; la mise en application des types d'organisation exigés par la norme ISO 9000 (page 43) ;
- le chapitre-4 (24 pages), fournit des notes d'application, en particulier à partir d'exemples portant sur l'utilisation de ces mémoires flash dans le cas des micro-processeurs 68000, pour lequel plusieurs diagrammes indiquent comment utiliser ce type de circuits mémoires. Ce micro-processeur utilise (voir page 47) 24 bits d'adressage pour le bus et 16 bits pour les données, avec 16 Méga bytes d'espace d'adresses des mémoires.
- le chapitre-5 (372 pages), décrit les caractéristiques individuelles pour les différents produits utilisant une alimentation en 5 volts ;
- le chapitre-6 (121 pages), décrit les caractéristiques individuelles pour les différents produits utilisant une alimentation en 3 volts ;
- le chapitre-7 (44 pages), décrit les caractéristiques individuelles pour les différents produits de type « cartes mémoires » où plusieurs circuits mémoires sont déjà assemblés pour constituer des mémoires de grandes capacités ;
- le chapitre-8 (39 pages), décrit les caractéristiques individuelles des différents modèles d'encapsulation des puces ;
- la dernière page est la liste des points de vente.

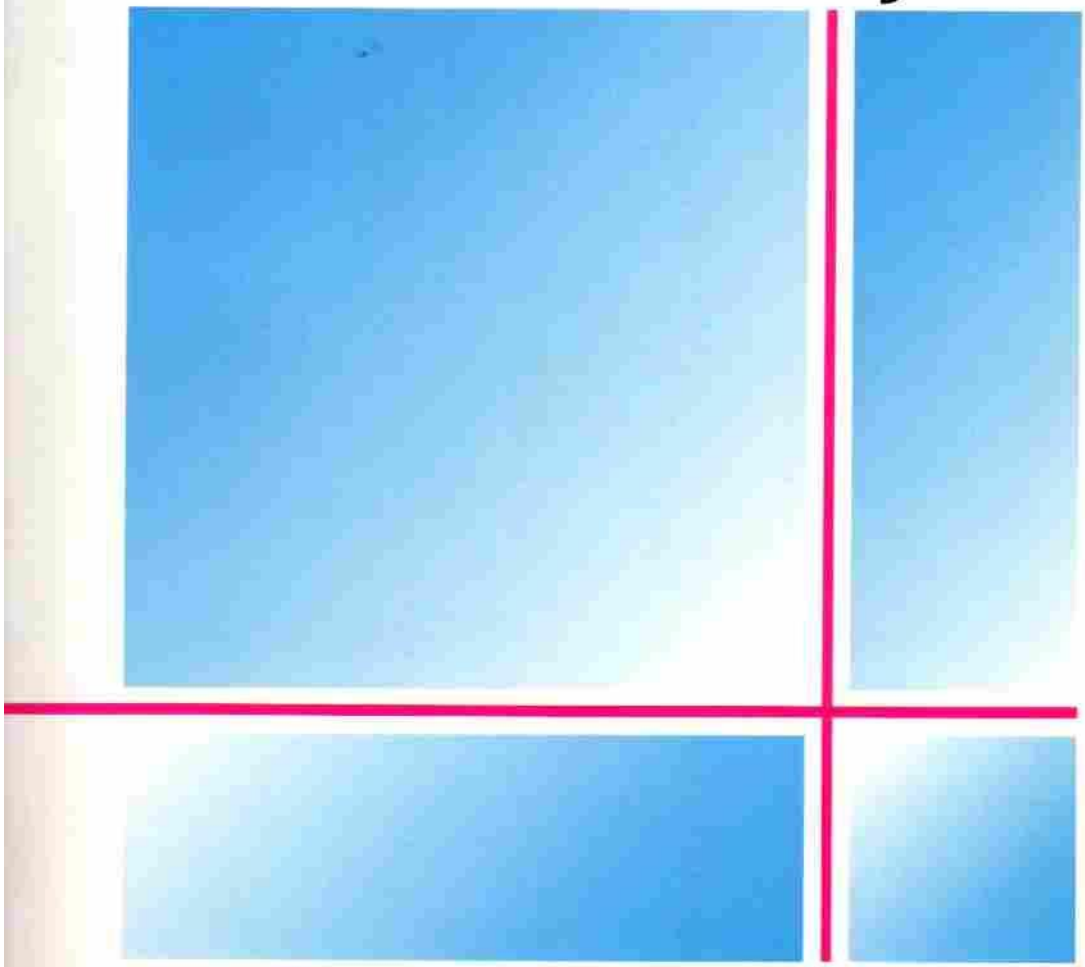
Le présent fichier PDF fournit quelques extraits des informations données par ce catalogue.

Pour utiliser ce document, mentionnez Fujitsu, ainsi que la Base de Données ACONIT n° 13666.

Fiche rédigée le 30/01/2019 par Jean Ricodeau.

FUJITSU SEMICONDUCTOR
DATA BOOK

1996/1997
Flash Memory



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Flash Memory Products

Fujitsu's Memory Products

Fujitsu's technological leadership in memory products is due to its responds to the market needs in developing products which will give customers that all-important competitive edge. Major investments in modern memory manufacturing facilities demonstrate Fujitsu's long-term commitment to the memory market.

The market for non-volatile memory devices, such as Flash memory products, is expected to show a significant growth in the next several years. To meet the future flash memory demand Fujitsu has entered into a 50/50 joint venture with AMD, incorporated in April, 1993 to produce non-volatile memory devices. Construction of its facilities was started in June, 1993 and completed in April, 1994. Fujitsu AMD Semiconductor Limited (FASL) is the real joint venture established under a close cooperative relationship of two leading semiconductor companies of the U.S. and Japan with distinguished technologies and expertise. FASL is engaged in a volume production of highly value-added semiconductor devices utilizing 8-inch wafers and design / process technologies capable of producing products with geometries of 0. 5 micron and smaller. The effort is to provide non-volatile memory products with worldclass quality and reliability to customers meeting their requirements.

FASL Facts:

Established	April 16, 1993
Mass-production start	February 1995
Location	Aizu-Wakamatsu, Japan
Floor space	26,000 square meters including 6,500 square meters clean room
Investment	2,0 Billion $ for Fab 1 and Fab 2

Preface

Preface

Fujitsu's Flash Memory products are based on a single-power-supply architecture of either 5 Volt-only or 3 Volt-only enabling low power consumption and cost reduction. This can be achieved by using a Negative Gate Erase technology and a NOR cell structure. The Flash Memories are manufactured in 0.5 µm CMOS technology, and due to technological progress also in 0.35 µm CMOS technology leading to smaller die sizes and faster data access times of a minimum of 55 ns. Low power consumption and guaranteed 100,000 write cycles are main characteristics of these products. Embedded Algorithms are a feature which simplify program and erase operations and increases endurance and reliability.

This Flash Memory data book introduces the flash memory technology and its application. An overview of the whole range of Fujitsu's flash memory products listing their key features is given. Fujitsu's dedication to quality and reliability to the manufacturing environment is characteristic to becoming a major supplier of flash memories. The data sheets of all available flash memories and flash memory cards are combined in this data book. Furthermore a introduction to packages and package outline diagrams are part of the package specification chapter. The reliability of the packages is fully assured through Fujitsu's Quality Assurance System.

For any questions regarding the specifications or descriptions in this Flash Memory data book, please contact the Fujitsu sales department or Fujitsu agent.

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Index

Cette page liste les produits du catalogue, et montre qu'un même composant peut intégrer des mémoires en 8 ou en 16 bits

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Flash Memory Product Range

Supply Voltage	Capacity	Organization	Part Number	Suffix	Access Time	Sector Architecture
Flash Memory / 5V ONLY	2M	256Kx8	MBM29F002T/B		90 to 120ns	Boot Block 1x16Kbyte, 2x8Kbyte, 1x32Kbyte, 3x64Kbyte
			MBM29F002ST/SB		90 to 120ns	Boot Block 1x16byte, 2x8byte, 1x32byte, 3x64byte
		256Kx8 128Kx16	MBM29F200TA/BA		70 to 120ns	Boot Block 1x16byte, 2x8byte, 1x32byte, 3x64byte
	4M	512Kx8	MBM29F040A	-X	70 to 120ns	Uniform Sectors 8sectors x 64byte
		512Kx8 256Kx16	MBM29F400TA/BA	-X	70 to 120ns	Boot Block 1x16byte, 2x8byte, 1x32byte, 7x64byte
	8M	1Mx8	MBM29F080	-X	90 to 120ns	Uniform Sectors 16sectors x 64Kbyte
		1Mx8 256Kx16	MBM29F800T/B		90 to 120ns	Boot Block 1x16Kbyte, 2x8Kbyte, 1x32Kbyte, 15x64Kbyte
	16M	2Mx8	MBM29F016	-X	90 to 120ns	Uniform Sectors 32sectors x 64Kbyte
3V ONLY	2M	256Kx8	MBM29LV002T/B		120 to 150ns	Boot Block 1x16Kbyte, 2x8Kbyte, 1x32Kbyte, 3x64Kbyte
		256Kx8 128Kx16	MBM29LV200T/B		120 to 150ns	Boot Block 1x16Kbyte, 2x8Kbyte, 1x32Kbyte, 3x64Kbyte
	4M	512Kx8	MBM29LV004T/B		120 to 150ns	Boot Block 1x16Kbyte, 2x8Kbyte, 1x32Kbyte, 7x64Kbyte
		512Kx8 256Kx16	MBM29LV400T/B		120 to 150ns	Boot Block 1x16Kbyte, 2x8Kbyte, 1x32Kbyte, 7x64Kbyte
	8M	1Mx8	MBM29LV008T/B		120 to 150ns	Boot Block 1x16Kbyte, 2x8Kbyte, 1x32Kbyte, 15x64Kbyte
			MBM29LV080		120 to 150ns	Uniform Sectors 16sectors x 64Kbyte
		1Mx8 512Kx16	MBM29LV800T/B		120 to 150ns	Boot Block 1x16Kbyte, 2x8Kbyte, 1x32Kbyte, 15x64Kbyte

Part Number
T: Boot block located at top address
B: Boot block located at bottom address
Suffix
None: Temperature range T_A=0°C to +70°C
-X: Temperature range T_A=-40°C to +85°C

1

Flash Memory - Background

3 Flash Memory- Background

Memories came into being only in the late 1960s emerging to a leading semiconductor component with multibillion dollar sales by today. By the end of the 1980s, the first flash memory devices have been introduced to the technical and scientific world by Toshiba in Japan, EXAR and Seeq Technology in the USA. However the breakthrough of these memories took place by the ISSCC (International Solid State Circuits Conference) of the IEEE in 1989, where the Flash memory announcement caused the strongest impact on the electronics industry.

The flash memory market is mainly driven by the PC and digital mobile phone industry. One reason for the necessity of flash memory was the shift from indoor to outdoor computing. The trend for portable equipment is to reduce weight and to save power therefore the need for small packages as well as for power saving semiconductors is given. As result, flash memory became the focus of attention offering a non-volatile storage medium requiring neither floppy disks nor disk drives.

5.0 Volt-only Flash Memory Negative Gate Erase Technology

4 5.0 Volt-only Flash Memory Negative Gate Erase Technology

Fujitsu's Negative Gate Erase, 5.0 V-only technology is the most cost-effective and reliable approach to single-supply Flash memories. The innovative approach Fujitsu has taken to 5.0 V-only technology provides designed-in reliability that is equal to that of its 12.0 V devices. In fact, transistor oxides are not subjected to any voltages higher than on Fujitsu's 12.0 V devices. This approach minimizes internal power generating requirements which results in a negligible impact on die size because of the 5.0 V-only reprogramming capability.

The minimal power requirement of Fujitsu's Negative Gate Erase, 5.0 V-only technology is made possible by design techniques which use the systems' Vcc power supply to provide the 10-20 mA (peak) current for Band-to-Band tunneling. Erase operations are performed when the system Vcc voltage is applied to the source terminal and the gate is pumped to a negative voltage. Less than 10 µA of current is required on the gate to enable Fowler-Nordheim tunneling.

Negative Gate Erase uses the same mechanism to erase a cell as the company's 12.0 V devices. Programming operations are performed with positive voltage pumped on the gate terminal at less than 10 µA of current. Hot channel electrons are injected into the floating gate in the same manner as 12.0 V devices.

The 5.0 V-only cell layout and geometry are comparable to the 12.0 V Flash memory cell. This ensures long term scalability equal to conventional 12.0 V flash designs without any penalty in die size. Fujitsu added Dual Layer Metal (DLM) technology to implement its flexible sector erase architecture. Fujitsu's unique sector isolation ensures reliable endurance cycling of at least 100K cycles for each sector whether erased individually or in combination.

Fujitsu's innovative charge pump design techniques allow this device to consume less power than 12.0 V devices during write operations. Approximately 90% charge pump efficiency is achieved with Fujitsu's unique diode V_t cancellation techniques. In addition, the charge pump design minimizes noise and ripple associated with voltage conversion circuits.

The culmination of these innovative design techniques makes this device ideal for power sensitive portable applications.

■ CHARGE PUMP CHARACTERISTICS — OVERVIEW

Before discussing the details of Fujitsu's 5.0 V-only technology it is helpful to review the basic concepts of charge pump design. These concepts apply to stand alone DC/DC converters as well as charge pumps integrated into the device silicon. All charge pump designs share common characteristics. For instance the available current from a voltage pump is determined by the Z_{out} and V_{out} of the circuit.

- Z_{out} is proportional to n/(C*F)
  - n = # of charge pump stages
  - C = capacitor size of each stage
  - F = clock rate
- Vout is proportional to n • (V_{CC} – V_{Diode})
  - n = # of charge pump stages
  - V_{out} = Device Vcc
  - V_{Diode} = voltage drop of charge pump blocking diode
- Noise is proportional to L • (di/dt)
  - L = bond wire inductance
  - di/dt = rate of current change

5.0 Volt-only Flash Memory Negative Gate Erase Technology

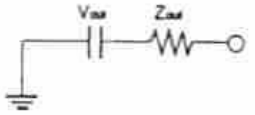
There are a number of issues to note about these relationships.

The silicon area of the charge pump is determined by the product of n and C (number of stages times the capacitor size). Efficient use of chip silicon requires this product to be as small as possible.

The efficiency of the voltage generated by the pump circuitry is increased as the effective voltage drop of the charge pump blocking diode is reduced ($V_{CC} - V_{Diode}$).

The voltage available at the output of the pump (when current is drawn) increases when Z_{out} decreases. Z_{out} decreases as either n is reduced or the product C*F increases. In addition, once a given Z_{out} is determined the values of C and F may vary in inverse proportion while maintaining the same product value.

Noise generated by the charge pump is minimized with a lower F (when n • C is large). But as F decreases C must increase in order to keep the product C*F constant.



Charge Pump Model

Negative Gate Erase Technology

Negative Gate Erase is used for erase operations in order to minimize the current drawn from the erase charge pump. In order to illustrate the importance of this, it is beneficial to first describe how today's 12.0 V V_{PP} Flash devices operate. Then conventional techniques of generating 12.0 V from a 5.0 V V_{CC} internally will be examined before discussing the benefits of Negative Gate Erase.

Today's 12.0 V Flash devices erase the memory cell at the Source terminal with 12.0 V applied. The gate is grounded and the drain is left floating. The external V_{PP} circuit supplies the V_{PP} current required for erase operations. This provides the 10-20 mA (peak) Band-to-Band tunneling current along with the Fowler-Nordheim tunneling current required to remove charge off the floating gate.

Conventional techniques in generating 12.0 V at the source terminal from a 5.0 V Vcc internal supply require huge charge pumps in order to supply the 10-20 mA (peak) of Band-to-Band tunneling current. This approach requires significant silicon real estate (charge pump area = n*C) and consumes large amounts of power [(12.0 V* 30 mA) ÷ Efficiency ≥ 360 mW].

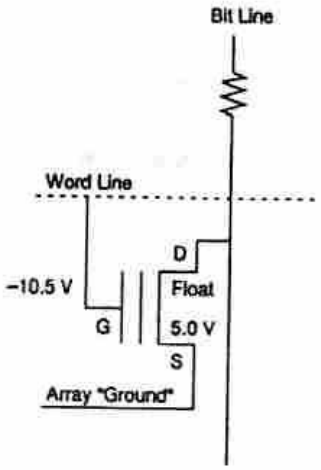
Multiple transistor EEPROM 5.0 V-only technology uses charge pumps to internally raise the gate voltages to between 18 and 20 V at < 10 µA. A multiple transistor approach requires one and a half to twice the silicon real estate as single-transister approaches. Both conventional 12.0 V Flash and Fujitsu's 5.0 V-only technology produce approximately half the electric field on the tunnel oxide as with EEPROM technology. The lower tunnel oxide fields extend the life of the oxide by orders of magnitude. In addition, EEPROM technology implements uniform channel tunneling instead of source-side tunneling as with conventional 12.0 V and Fujitsu's 5.0 V-only technology. Uniform channel tunneling stresses the entire oxide region while source-side tunneling only stresses a small region of the oxide.

Fujitsu's Negative Gate Erase technique actually provides the same electric fields to the Flash memory cell and uses the same erase mechanisms as its 12.0 V Flash devices. Negative Gate Erase is used in order to reduce the current drawn from the erase charge pump. The Band-to-Band tunneling current (10-20 mA peak) comes directly from the system Vcc through the Array Ground terminal. This is the most efficient way to use an existing system Vcc supply. The current required from the Negative Gate Erase charge pump is less than 10 µA at −10.5 V. This

5.0 Volt-only Flash Memory Negative Gate Erase Technology

reduces the internal power consumption in relation to conventional 12.0 V approaches.

A circuit diagram of Negative Gate Erase is illustrated below.



5.0 V-Only Negative Gate Erase Circuitry

Notes:

1. Gate terminal is pumped to −10.5V @ < 10 mA current
2. 10 mA – 20 mA (peak) erase current is provided to the Source terminal by the system's Vcc supply.

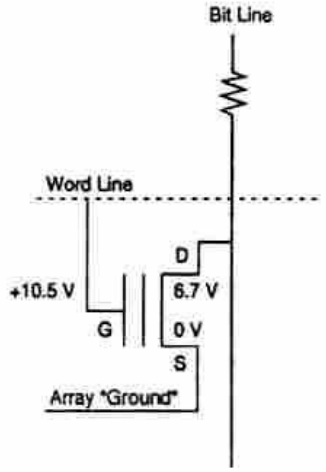
Key:
D = Drain terminal
G = Gate terminal
S = Source terminal

■ 5.0 V-ONLY PROGRAMMING

Fujitsu's 5.0 V-only programming technique provides the same electric fields to the memory cell and uses the same programming mechanisms as its 12.0 V Flash devices. The drain is pumped to 6.7 V from 5.0 V and supplies approximately 0.5 mA of current per cell. The internal power generation required for the Channel Hot Electron injection mechanism is minimized because the charge pump only delivers a 34% voltage increase from the base Vcc supply. This also provides the benefit that the cell's programming characteristics remain constant even if the system Vcc supply varies. This current supplies the Channel Hot Electrons that are injected into the floating gate in order to program the memory cell. The current required by the gate voltage charge pump is less than 10 μA. This minimizes internal power consumption.

A circuit diagram of the programming circuitry is illustrated below.

5.0 Volt-only Flash Memory Negative Gate Erase Technology



5.0 V-only Drain Programming

Notes:

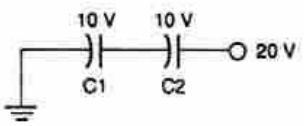
1. Gate terminal is pumped to –10.5V @ < 10 mA current
2. Drain terminal is pumped to 6.7 V from 5.0 Vcc supply @ 0.5 mA.

■ FUJITSU'S 5.0 V-ONLY DEVICE EQUALS THE RELIABILITY OF 12.0 V DEVICES

Equivalent Electric Fields Charge Pump Circuitry

One component of device reliability is related to the electric fields applied across internal device transistors. Very high electric fields may cause oxide breakdown and hence reliability problems. One of the main design and reliability requirements in Fujitsu's 5.0 V-only circuit implementation was the maintenance of electric fields across the charge pump oxides equivalent to those of the oxides subject to high voltage in the 12.0 V device. Fujitsu's techniques minimize the electric fields across the oxides to be equivalent to those across the device transistor oxides during standard Read operations of the 12.0 V device. This ensures that the 5.0 V-only design will not be more susceptible to oxide failures than 12.0 V devices. There has never been any physical damage to an oxide from the high voltages internal to Fujitsu's 12.0 V Flash device.

One way to maintain low electric fields across transistor oxides is to stack multiple capacitors together. This circuit technique delivers a large output voltage while maintaining low electric fields across each oxide. As an example, with an oxide that is able to reliably withstand voltages of 10 V, a circuit can be constructed to provide 20 V by stacking (in series) two capacitors with 10 V across each oxide. This circuit ensures that the electric fields remain within the specified limits.



Capacitators Charge Pump Model

5.0 Volt-only Flash Memory Negative Gate Erase Technology

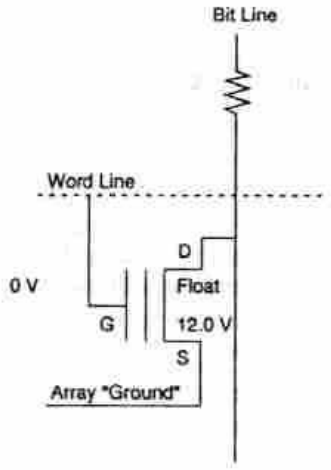
Memory Cell Circuitry

It is important to note that the electric fields applied to the data storage memory cells of the 5.0 V-only device are the same as that of the 12.0 V device. This ensures that the 5.0 V-only design will not be more susceptible to oxide failures than 12.0 V devices. An observable measure that the electric fields are indeed the same is found in the erase time parameter. Erase time depends upon the electric field across the floating gate and the thickness of the tunnel oxide (Tox). Tox and the erase time of the 5.0 V-only device are the same as in the 12.0 V device. Therefore the electric field is the same in both devices.

The electric fields of the 5.0 V circuit are also demonstrated by analyzing the coupling ratios in the memory cell transistor. However, it is first beneficial to discuss the coupling ratios of standard 12.0 V Flash circuitry. We will use the erase circuit as an example. The same concepts apply to the programming circuitry.

Electric Fields in Standard 12.0 V V_{PP} Erase Circuits

The standard Flash memory cell applies 12.0 V to the Source terminal. The Gate terminal is grounded and the drain is left floating. The actual electric field seen by the tunnel oxide is a superposition of three components. One is because the field generated by the trapped electrons on the floating gate. This is the state of a programmed memory cell prior to erase. The other two result from coupling of the voltage between the word line (Gate terminal)/ floating gate and between the source terminal/floating gate. In the case of standard 12.0 V V_{PP} programming, the only component from the voltage coupling is between the source terminal and the floating gate. There is no coupling from the word line because it is at a zero voltage potential. The resulting electric field never exceeds a peak value of 10 mV/cm.



Standard 12.0 V V_{PP} Erase

Notes:

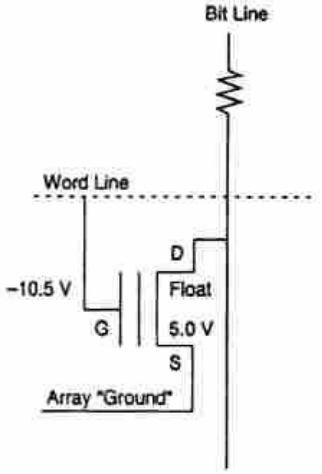
1. Tunnel oxide (Tox) electric field is determined by super-position.
   - Floating Gate Voltage from stored electrons reduces voltage across Tox
   - Source Coupling Voltage on the floating gate reduces the voltage across the Tox
2. Total electric field acrss Tox due to superposition is < 10 mV/cm.

5.0 Volt-only Flash Memory Negative Gate Erase Technology

Equivalent Electric Fields in Fujitsu's 5.0 V-only Negative Gate Erase Circuitry

Fujitsu's Negative Gate Erase circuitry applies the same electric fields to the memory cell as the 12.0 V device. The Gate terminal is negatively pumped to −10.5 V and the source terminal is at 5.0 V supplied by the system Vcc supply. The drain terminal is left floating. The actual electric field seen by the tunnel oxide is a superposition of three components. One is due to the field generated by the trapped electrons on the floating gate. This is the state of a programmed memory cell prior to erase. The other two result from coupling of the voltage between the word line (Gate terminal)/floating gate and between the source terminal/floating gate. This time there is voltage coupling from both the Source terminal and word line. The resulting electric field is the same as in the 12.0 V device. The electric field is always ≤10 mV/cm.

In addition, the Negative Gate Erase approach actually produces a lower electric field across the cell junctions. This is because the source terminal is subjected to 5.0 V levels instead of 12.0 V.



5.0 V-only Negative Gate Erase

Note:

1. Tunnel oxide (Tox) electric field is determined by superposition.
   - Floating Gate Voltage from stored electrons reduces the voltage across Tox
   - Gate Coupling Voltage on the floating gate reduces the voltage across the Tox
   - Source Coupling Voltage on the floating gate reduces the voltage across the Tox
2. Total electric field across Tox due to superposition is < 10 mV/cm.

■ DATA INTEGRITY

Ruggedized Programmability

Fujitsu's 5.0 V-only approach is designed not to be sensitive to variations in the system Vcc supply during programming operations.

This is achieved by pumping the drain terminal to 6.7 V. The device actually compensates for any system level variations in the Vcc supply. During programming the word line is pumped to +10.5 V and the source terminal is grounded. These voltage conditions and resulting electric field are the same as in 12.0 V devices.

5.0 Volt-only Flash Memory Negative Gate Erase Technology

Sector Write Protection

Fujitsu implements a Dual Layer Metal (DLM) bussing technique in order to provide the most cost-effective and reliable method to individually isolate sectors during sector erase operations. This technique inhibits the presence of high voltage in non-addressed sectors from disturbing fixed data. Data in non-addressed sectors is isolated from all other sector program and erase operations.

■ MINIMIZING CHARGE PUMP NOISE AND VOLTAGE RIPPLE

Minimizing Noise

Fujitsu's charge pump circuitry minimizes noise with a multi-stage pump design. Each stage has the same clock rate but is out of phase with all other stages. The phase shifting minimizes potential noise from any of the individual pumps. This technique delivers a very smooth and constant source of power. A V-8 automobile engine serves as an excellent analogy. Each of the eight stages of the charge pump is 45° out of phase. Each packet of charge is delivered in a way to provide a smooth flow of current.

Achieving 100,000 Cycle Endurance: A Report on Flash Endurance and Reliability

5 Achieving 100,000 Cycle Endurance: A Report on Flash Endurance and Reliability

This article discusses the Advanced Micro Devices approach to achieving and guaranteeing superior Flash endurance. The data presented will prove that Fujitsu's 100,000 cycle Flash devices provide the highest endurance and reliability levels in the industry.

Today's typical Flash applications are perfectly suited to 10,000 cycle endurance devices. This industry standard level of endurance is appropriate for applications such as PC BIOS and other designs that require infrequent code updates. At the same time, new Flash applications are currently being developed which require data to be reprogrammed more than 10,000 times. For applications of this sort, such as solid state hard disks, industry standard Flash devices cannot be counted on to performs reliably. Fujitsu has revolutionized this segment of the Flash market with the new Embedded Program™ and Embedded Erase™ Algorithms, which guarantee 100,000 write/erase cycles.

■ WHAT IS ENDURANCE?

Endurance is a popular term in the Flash industry. What exactly does endurance mean, and how should it be measured?

Fujitsu defines *endurance* as the number of write/erase cycles a Flash device can withstand without failure. Endurance must be measured under the worst-case conditions of the system environment, in order to guarantee products which operate across the range of data sheet specifications.

Understanding endurance is essential for Fujitsu, in order to manufacture superior Flash devices. Flash consumers must also understand the issues involved in achieving and guaranteeing endurance, so that they are assured of choosing the best devices on the market. In particular, consumers whose designs require extended endurance, i.e., more than 10,000 cycles, should be especially concerned with these issues.

Two failure modes are typically associated with Flash memories: hard failures and soft failures. *Hard failures* are complete and unrecoverable, and their root cause lies in the manufacturing process. Closely controlled manufacturing processes eliminate hard failures in Fujitsu's Flash devices, increasing the level of device quality and reliability.

Flash memory endurance is typically limited by *soft failures*. Soft failures occur when random bits erase too quickly. Flash memories are erased in blocks, and since not all bits exhibit identical erase characteristics, a fast-erasing bit must be exposed to the erase voltage until the slowest bit is erased. As a result, the fast bits can be erased "too much," forcing the transistor cells into depletion mode. This condition is called *over-erase*. An over-erased bit produces a *leakage current* which causes an entire column to malfunction. The result seen by the user is a system failure.

■ FUJITSU'S EMBEDDED ALGORITHM: THE KEY TO EXTENDED ENDURANCE

The soft failures described above occur in all Flash memories. These failures are precisely the reason that today's Flash devices are currently limited to 10,000 cycles. Applications which perform more than 10,000 write/erase cycles may jeopardize system reliability if standard rated 10,000 cycle Flash devices are designed in.

Now, Advanced Micro Devices makes extended endurance Flash applications possible with the introduction of the Embedded Program and Embedded Erase Algorithms. Fujitsu's Embedded Algorithm incorporates a function which *seeks out* and *corrects soft failures*, allowing these devices to be guaranteed for *100,000 write/erase cycles* (actual device performance may be orders of magnitude greater). The Embedded Algorithm extends endurance by

Achieving 100,000 Cycle Endurance: A Report on Flash Endurance and Reliability

automatically recovering over-erased bits, making soft failures transparent to the system. Flash devices that do not support these algorithms are incapable of recovering soft failures; thus, they cannot guarantee 100,000 write/erase cycle endurance. Only Fujitsu offers this self-correcting mechanism that makes extended endurance Flash applications possible.

■ FAILURE RATE COMPARISON

Figure 1 illustrates Fujitsu's significant endurance advantage over other standard rated 10,000 cycle Flash products. The graph shows that the endurance of Fujitsu's 100,000 cycle Embedded Algorithm devices represent a significant breakthrough in Flash endurance, as illustrated by the nearly flat failure rate curve.

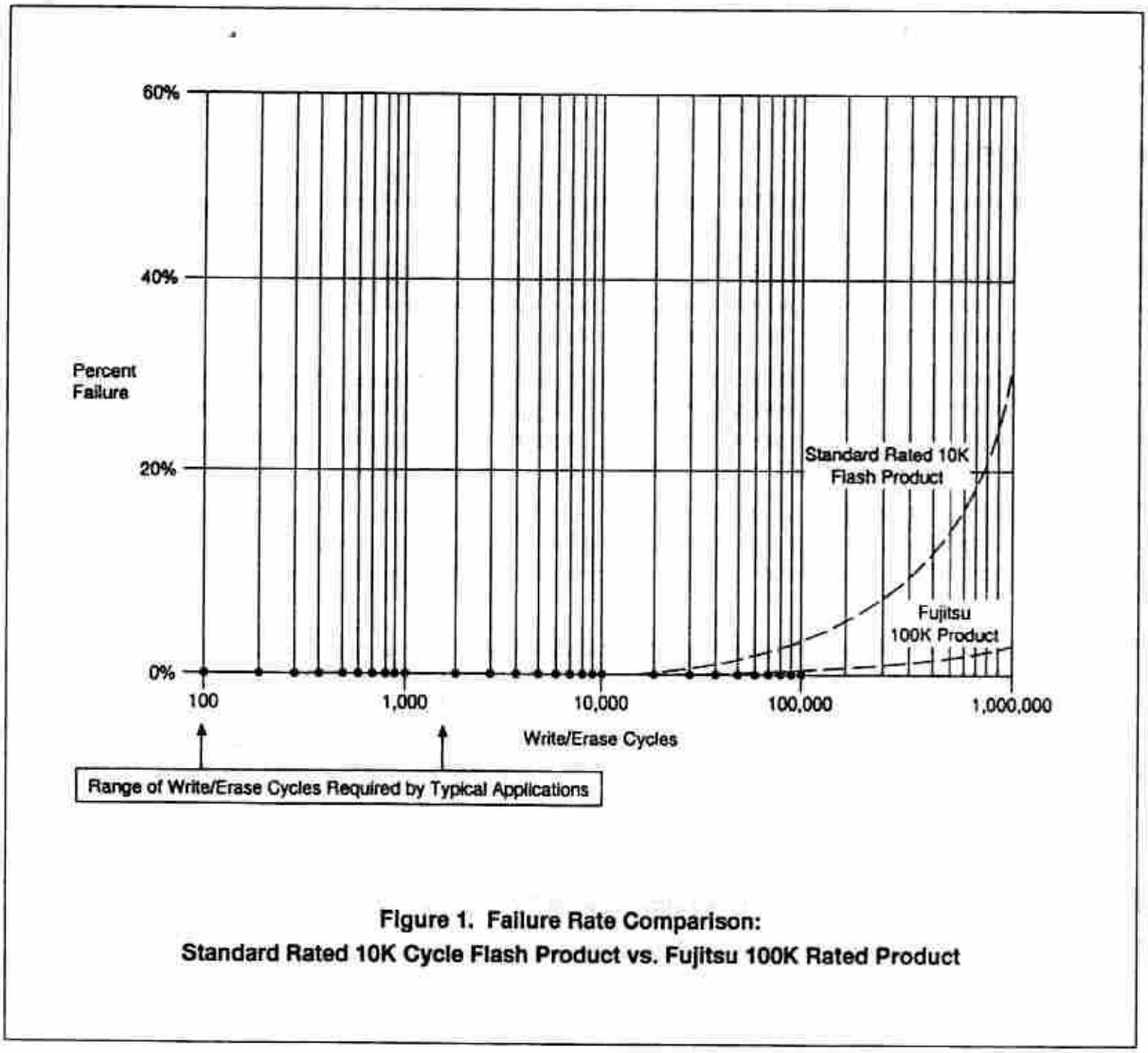


Figure 1. Failure Rate Comparison:
Standard Rated 10K Cycle Flash Product vs. Fujitsu 100K Rated Product

Achieving 100,000 Cycle Endurance: A Report on Flash Endurance and Reliability

Fujitsu's Embedded Algorithm devices represent a significant technology advancement in Flash endurance.

Test results prove that Fujitsu's Flash technology produces superior endurance. As Table 1 shows, the endurance failure rate at 100,000 cycles for Fujitsu's Embedded Algorithm devices is less than 0.25%.

Table 1. Fujitsu Embedded Algorithm Endurance Data

Device	No. of Lots	Initial Qty	Failures@			
			10K	25K	50K	100K
MBM28F010A	5	1159	0/1159	0/445	0/445	1/445
MBM28F020A	2	420	2/420	1/418	0/248	0/248

■ ENDURANCE AND RELIABILITY

Endurance and reliability are equally important issues, though not exactly synonymous. Reliability refers to the absence of hard failure mechanisms, which can be eliminated during processing. Fujitsu's Flash manufacturing processes are carefully controlled to produce products with immunity from hard failures. Endurance, as discussed earlier, relates to the occurrence of soft failures. Fujitsu's Embedded Algorithm guarantees superior endurance by correcting soft failures in-system.

Fujitsu understands that from a customer's perspective, all failures are unacceptable, regardless of their cause. For this reason, Fujitsu's Flash devices combine unsurpassed reliability and endurance for protection against hard failures as well as soft failures. Reliability tests show that Fujitsu's Flash process technology provides unmatched immunity from hard failures: *less than 10 FITs* on both High Temperature Operating Lite (HTOL 150°C, Vcc = 6.5 V) and Data Retention Bake (DRB 150°C, unbiased) using the 60% UCL calculation at 55°C.

Reliability data also prove that Fujitsu's unparalleled endurance is achieved without sacrificing reliability HTOL and DRB reliability tests were performed on the same Embedded Algorithm devices that had been cycled 100,000 times. *Table 2 shows that even after 100,000 cycles, there were NO reliability failures.* Flash endurance and reliability are two distinct and important issues, and the data proves that Fujitsu is superior in both.

Table 2a. Unbiased DRB @ 150°C after 100,000 Write/Erase Cycles

Device	Initial Qty	Failures@			
		48 Hrs	168 Hrs	500 Hrs	1000 Hrs
MBM28F010A	100	0/100	0/100	0/100	0/100

Table 2b. HTOL Reliability Results @ 6.5V Vcc, 150°C after 100,000 Write/Erase Cycles

Device	Initial Qty	Failures@			
		48 Hrs	168 Hrs	500 Hrs	1000 Hrs
MBM28F010A	180	0/180	0/180	0/180	0/180

FUJITSU

Achieving 100,000 Cycle Endurance: A Report on Flash Endurance and Reliability

Fujitsu is the technology leader in Flash memories. At the 10,000 cycle level, Fujitsu offers devices compatible with the industry standard. At the 100,000 cycle level, Fujitsu's Embedded Algorithm devices are unmatched in the industry, truly guaranteeing 100,000 cycle endurance.

For leadership in higher endurance, reliability, and quality in Flash memories, look to Fujitsu: your Flash leader!

For further information, please contact your local Fujitsu sales representative.

Embedded Algorithms in Flash Memories

6 Embedded Algorithms in Flash Memories

Application Note by Mike Harris

Despite their instant popularity, the first 12.0 V Flash memories introduced in the late 80s had several drawbacks. One of the concerns most often voiced by system software designers was the need for cumbersome programming sequences to program and erase the devices. Embedded Algorithms were developed to eliminate these concerns.

■ THE DRAWBACKS OF PROGRAMMING WITH FIRST GENERATION ALGORITHMS

Figure 1 shows the flowchart for programming Flash devices using first generation algorithms. The steps needed to program a single byte of memory are illustrated in simplistic block diagram form. The programming code itself is obviously much more complex. The erase sequence is similar except Flash devices must first be programmed to all zeros prior to being erased.

A completed listing of code performing all of the program/erase functions for a Flash memory typically contains 100-200 lines. Although sample code can be obtained from the device manufacturer, designers usually need to generate their own code specific to the individuality of their application.

This extensive programming requirement has many disadvantages and can be quite costly. First, of course, is the amount of time required to generate and debug this code. Since prior designs utilizing EPROMs were programmed offline, most software engineers are not familiar with the programming of Flash memories. They find that the programming process is initially lengthy and error prone. The cost to the user includes not only the obvious cost of software development but also the lost opportunity costs resulting from time to market delays.

Another concern is the potential long term impact on system reliability caused by overstressing a Flash device. Since cycling endurance can be affected by improper writing or erasing, software bugs can cause latent field failures even in systems that appear error free in development. In fact, most customer returns at Fujitsu have been traced to software errors generated during system development.

Embedded Algorithms in Flash Memories

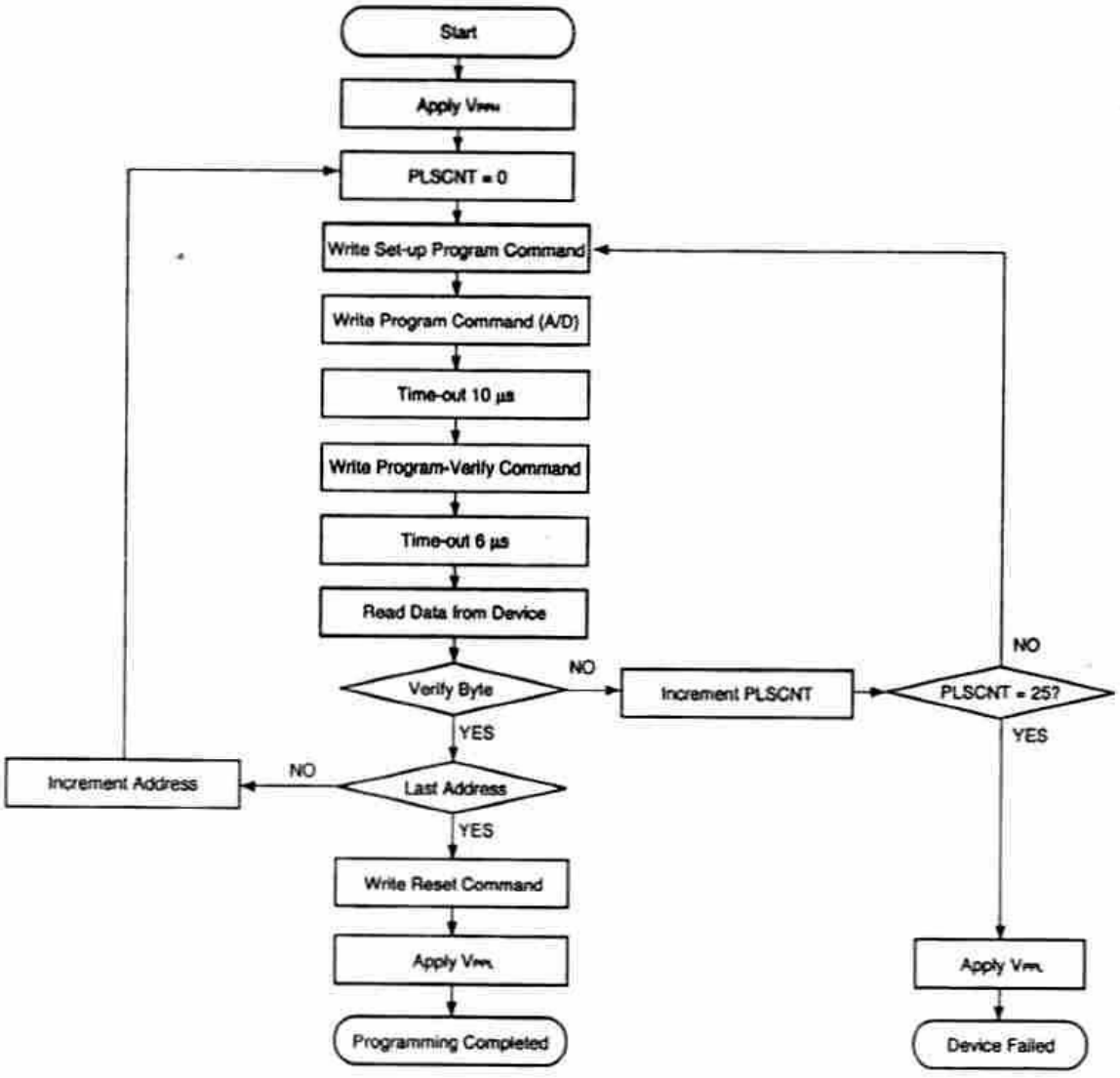


Figure 1. First Generation Programming Algorithm

Embedded Algorithms in Flash Memories

■ SIMPLIFYING FLASH PROGRAMMING

Fujitsu was the first company to recognize the need to simplify programming of Flash memories and incorporated it in the design of its first 2 Mbit Flash memory. Figure 2 illustrates the Embedded Program™ Algorithm. The system processor simply issues the write set-up command followed by the write command and the internal state machine on the device takes over control of the write operation. The system processor simply does $\overline{\text{DATA}}$ polling until the device indicates that the write operation is complete. This simplicity is even more pronounced during an erase operation since each byte of the memory must be individually programmed prior to erase. The Embedded Erase™ Algorithm internally writes all zeros to each byte and then performs the erase. This entire sequence is controlled internally and is transparent to the host processor.

■ OTHER ADVANTAGES OF EMBEDDED ALGORITHMS

Besides simplifying the complex programming of Flash memories, Embedded Algorithms offer these other important advantages to the designer:

Reduced system overhead — Since the Embedded Algorithms are completely automatic, the system processor is free to perform other functions, such as servicing interrupts, during the write or erase operations.

Improved program/erase time — The Embedded Algorithms are designed to perform write/erase operations in the most efficient way possible. All system overhead is eliminated.

Increased cycling endurance — By including a self correcting mechanism, Flash memories incorporating Fujitsu's Embedded Algorithms will operate to a minimum of 100,000 endurance cycles.

JEDEC standards for self programming of Flash devices are now being developed. The Embedded Algorithms incorporated in all of Fujitsu's Flash devices conforms to these standards.

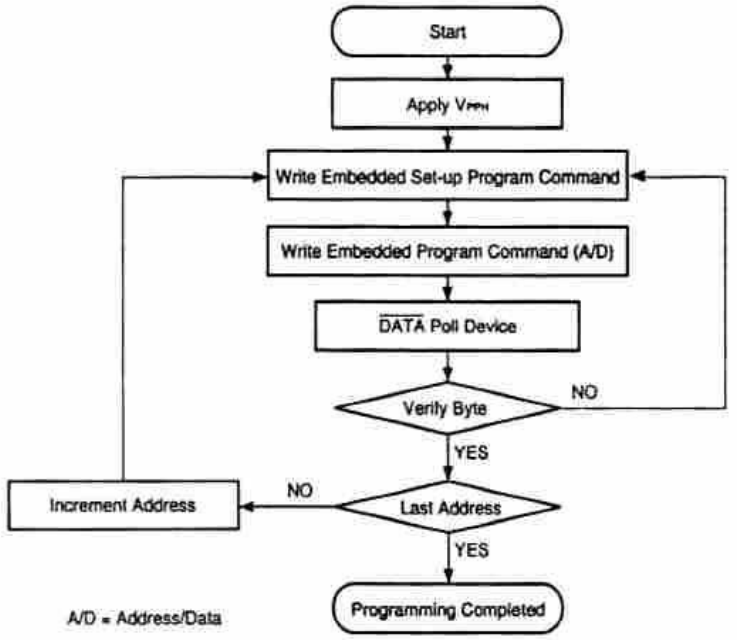


Figure 2. Embedded Programming Algorithm

FUJITSU

Embedded Algorithms in Flash Memories

■ SUMMARY

The benefits of Embedded Algorithms are available from Fujitsu on 5.0 Volt-only and 3.0 Volt-only devices, fully sectored MBM29F and MBM29LV family. Employing these algorithms in existing designs will allow you to increase your system's endurance to over 100K cycles. In new designs, system development will be simplified and time to market reduced.

Fujitsu Reliability and Quality Program

The Fujitsu Philosophy for Quality and Reliability

Fujitsu components are renowned the world over for their outstanding quality and reliability. In Fujitsu, we believe that three factors contribute to this achievement: **the people, the process and the products.**

The People: Quality created by highly motivated staff

Not only are our staff members highly skilled in all aspects of process management and control, they are also totally dedicated to achieving the very highest standards of quality and reliability.
This is due to Fujitsu's special personnel training where each and every individual employee is fully aware of the importance of his or her task to the achievement of quality in the end products.

The Process: Quality built into every stage

Maintaining the production process in optimum working order is the key to high yields and a dependable supply to quality semiconductors.
At Fujitsu, this is achieved by exhaustive checks and stringent quality standards at each stage of the manufacturing process, from product definition right through to final delivery.

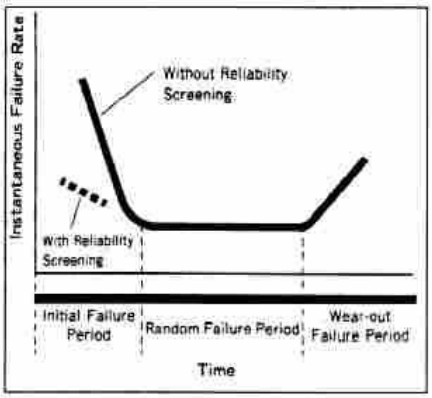
The Products: Reliability for all of society

Fujitsu's experience as a major supplier of computers and communications equipment leads to us developing the right products for our customer's needs.
Reliable components lead to reliable end products and this contributes to the growth and prosperity of our many customers and of all those people who use our products.
This is Fujitsu's goal.

Fujitsu Reliability Program

Reliability Screening

Distribution of Component Failure



The failure rate for semiconductors usually follows the kind of 'bathtub curve' shown in the figure. The many tests and inspections during the manufacturing process manage to eliminate almost all the factors that cause rejects. Nevertheless a few defective products still pass.
Fujitsu's reliability screening process subjects these products to additional stress before shipping. This process eliminates more defects after a short period of operation in the field, the so called 'Infant Failures'. We reduce the number of initial defects by carefully controlling the production process and building quality into every step of production.
By including a burn-in in the screening process, the Infant Failures can be removed and the remaining devices have a very low chance of field failure.
VLSIs are achieving ever higher densities on submicron design levels. Thus this screening process has become essential for reducing defects in the early stages of manufacture.

Reliability Monitoring

After mass production, lot reliability tests and other regular reliability tests (see the table) confirm product reliability. Products are classified into families according to their circuit functions and processes. Each family provides samples for testing as shown in the tables.

Example of Sampling Plan for Reliability Testing

Environmental Tests

Test Items	Device		Module		Memory Card		* Note
	Sample Size	Acceptance Number	Sample Size	Acceptance Number	Sample Size	Acceptance Number	
Temperature Cycle	55	0	11	0	11	0	These tests take 100 cycles.
Thermal Shock ※1	25	0	11	0	25	0	These tests take 100 cycles.
PTHS ※2	55	0	11	0	—	—	These tests take 168 hours.
PTHB ※2	25	0	—	—	—	—	These tests take 96 hours.

Endurance Tests

Test Items	Device		Module		Memory Card		Note
	Sample Size	Acceptance Number	Sample Size	Acceptance Number	Sample Size	Acceptance Number	
High-Temperature Storage	25	0	11	0	25	0	These tests take 1,000 hours.
Operating Life Test	55	0	—	—	25	0	
High-Humidity Bias ※2	25	0	—	—	25	0	

※1: Ceramic Package only ※2: Plastic Package only

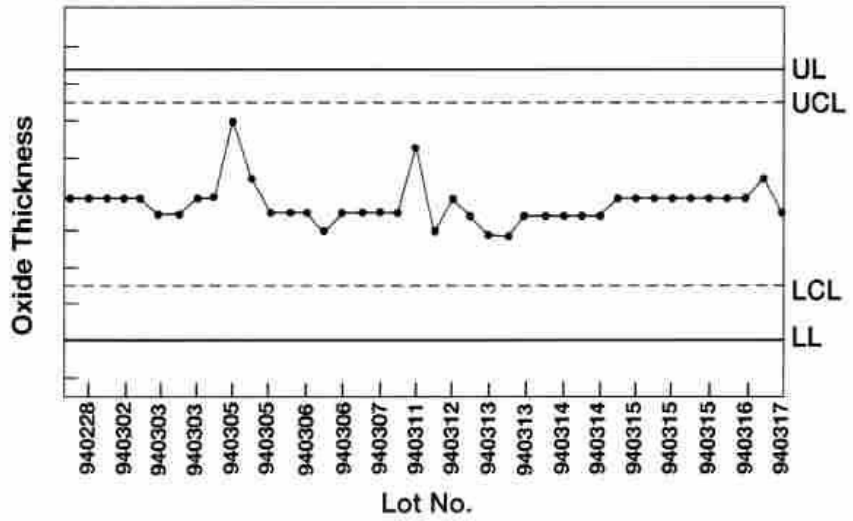
Fujitsu Quality Program

In-Process Manufacturing Groups Inspections
Fujitsu's Manufacturing Groups implement these inspections to set control items and standards for each manufacturing process. Prompt feedback maintains and improves the quality consciousness throughout the groups.
Inspection occurs regularly for each lot and/or each production line.

In-Process QC Groups Inspections
The Quality Control Groups inspect at the end of major manufacturing phase.
Using the sampling standards, the groups confirm the level of quality before the products proceed to the next phase.

Statistical Process Control (SPC)
Fujitsu's SPC program uses statistical analysis. Engineering Groups set the major quality parameters and their spec value for the manufacturing processes to assure the proper quality. The Manufacturing Groups determine the control values for the equipment and conditions for the production process.
Once mass production begins, the Manufacturing Groups implement control plans to check and improve the product capability of each process.
Some important parameters are film thickness, monitor characteristics, bonding strength, electrical characteristics and yield (see figure below). Computer software checks each parameter automatically.

16M DRAM Oxide Thickness

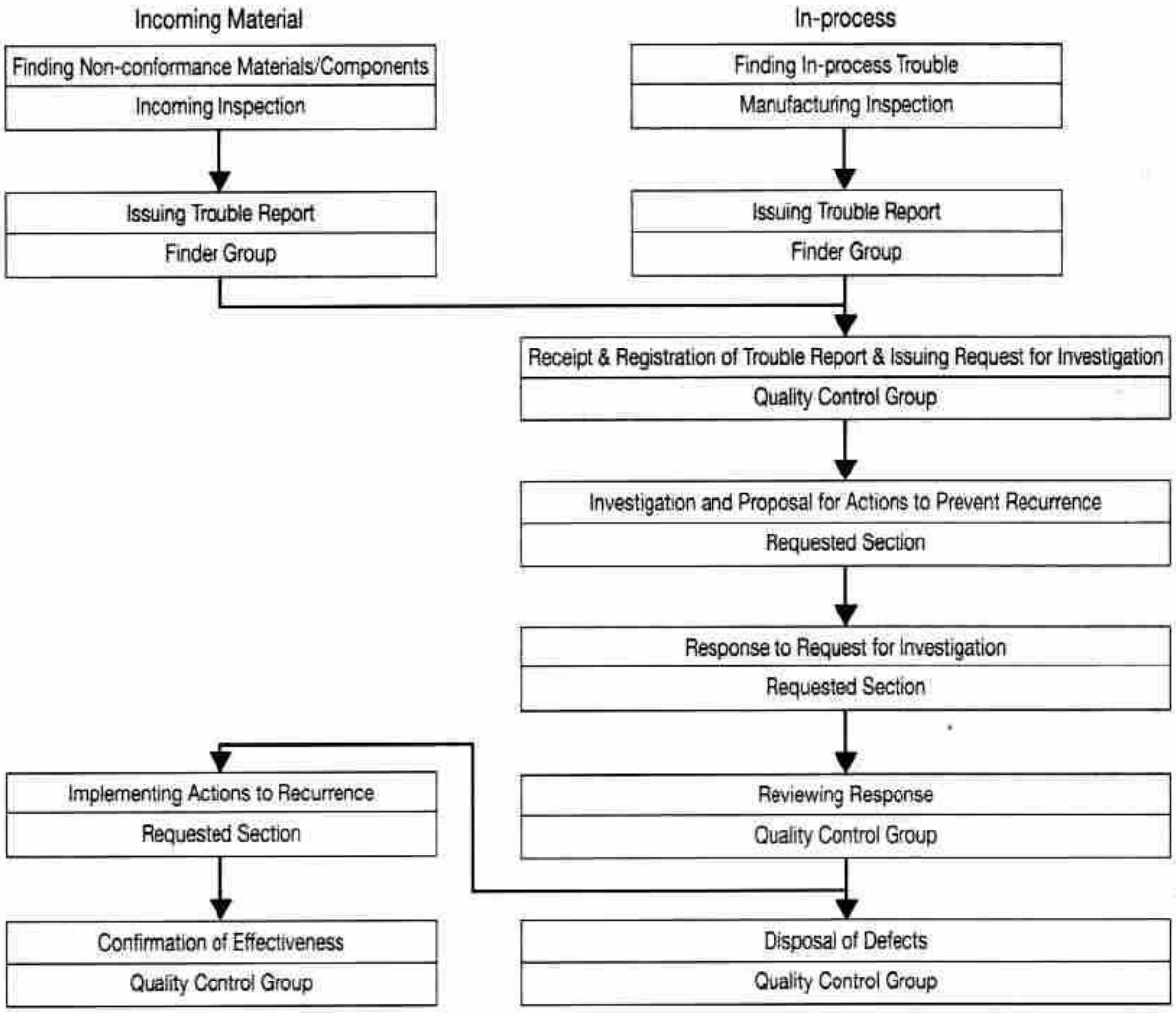


Support for Quality and Reliability

In-Process Troubleshooting

Whenever a problem arises that might interfere with the manufacturing process, we immediately investigate the cause, select and implement countermeasures, and take steps to suppress the problem. The QC Group confirms that the countermeasures are effective.

In-Process Troubleshooting Flow



Sharing Information

We share the data from our in-house-company mass production approval tests with our customers. Whenever possible, we also provide our customers with test results that are not part of our normal test package.

Dock to Stock

To supply our products quickly and to reduce the costs to our customers, we have implemented a 'dock to stock' system. This system informs our customers of the results of our shipping and reliability tests.

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Support for Quality and Reliability

Engineering Change Notification
Occasionally advances in manufacturing technology will cause engineering changes in our product specifications. When a change might affect the properties, quality, or reliability of a product, we notify the customer the change, if necessary.

Plant Audit
We believe that regular plant inspections are an ideal way to build good relations with our customers. We respond eagerly to customer requests to visit our plants because such visits help us to understand our customer's needs better and to incorporate those needs into manufacturing process.
Excellent semiconductors can only be made at well-equipped plants. At Fujitsu, we are proud of the advanced level of our manufacturing methods.

Document Control
Fujitsu's standards govern all specifications sheets. The group responsible for the specification prepares or revises each document.
The Spec Control Group supervises issuance and maintenance of there original spec sheets. This group has total control over documents. It keeps records on the number and destinations of the distributed spec sheets.
When we receive 'special' requests, the Engineering Support Group issues a Spec Action Request (SAR, see figure). Based on this SAR the Engineering Group then incorporates this special request and adapts the revised procedure to the manufacturing process.

In-Line Audit
The Quality Control Group at every Fujitsu plant regularly audits the quality and reliability control in all groups at the plant. The QC group uses a comprehensive checklist prepared by our company to evaluate the audit and take appropriate measures to correct any problems. The items on the checklist include the following:

- In-process inspections (including in-coming inspections and shipping tests).
- Systems for approvals and quality checks.
- Education and training.
- Document control.

Support for Quality and Reliability

Approval for International Organization for Standardization (ISO)

Fujitsu has a clear concept to approve the ISO9000 series.

Fujitsu ISO9000 Series Approval Status

Plants have been already Approved ISO9000 Series

	No.	Plant Name	Certification Body	ISO9000 Series	Approval Date	Certification Number
	1	Kawasaki Plant	JQA	ISO9001	1994.12.22	JQA-0711
	2	Mie Plant	JQA	ISO9002	1994.02.21	JQA-0412
	3	Aizuwakamatsu Plant. Aizu Plant	JQA	ISO9002	1994.03.14	JQA-0440
	4	Aizuwakamatsu Plant. Wakamatsu Plant	JQA	ISO9002	1994.03.08	JQA-0426
	5	Iwate Plant.	JQA	ISO9002	1994.03.29	JQA-0450
※1	6	KFJ Kagoshima Division.	JQA	ISO9002	1993.12.21	JQA-0351
※2	7	KFJ Miyazaki Division.	JQA	ISO9002	1993.09.13	JMI-0270
※3	8	FJM	JQA	ISO9002	1993.11.24	JQA-0325
※4	9	FTE	JQA	ISO9002	1993.12.02	JQA-0336
※5	10	FVD Gifu Division	JQA	ISO9002	1993.12.15	JQA-0342
※6	11	FVD Kohzohji	JQA	ISO9001	1994.11.11	JQA-0662
※7	12	FQD	JQA	ISO9002	1993.09.17	JMI-0278
※8	13	FME (Ireland)	NSAI	ISO9002	1993.07.03	M929
※9	14	FMAL (Singapore)	SGS Yarsley	ISO9002	1993.05.27	SGS93/1915
※10	15	FMM (Malaysia)	SGS Yarsley	ISO9002	1993.08.23	SGS93/2207
※11	16	FML (Durham)	SGS Yarsley	ISO9002	1992.11.11	SGS92/1348
※12	17	FMG (Germany)	DQS	ISO9001	1994.11.16	2802-01
※13	18	FMI (Gresham)	TÜV	ISO9002	1995. 06.23	74 100 5538
※14	19	FDI	JQA	ISO9001	1995. 05.12	JQA-0873

※JMI was changed in 1993.10.01 (JQA: Japan Quality Assurance Organization).

※1	KFJ	Kagoshima Division	:	Fujitsu Kagoshima Electronics Ltd.
※2	KFJ	Miyazaki Division	:	Fujitsu Miyazaki Electronics Ltd.
※3	FJM		:	Fujitsu Miyagi Electronics Ltd.
※4	FTE		:	Fujitsu Tcuhoku Electronics Ltd.
※5	FVD	Gifu Division	:	Fujitsu VLSI Ltd.
※6	FVD	Kohzohji Headquarters	:	Fujitsu VLSI Ltd.
※7	FQD		:	Fujitsu Quantam Devices Ltd.
※8	FME	(Ireland)	:	Fujitsu Microelectronics Ireland Ltd. Ireland Plant
※9	FMAL	(Singapore)	:	Fujitsu Microelectronics Asia PTE. Ltd. Singapore Plant.
※10	FMM	(Malaysia)	:	Fujitsu Microelectronics Asia SDN. BHD. Malaysia Plant.
※11	FML	(Durham)	:	Fujitsu Microelectronics Ltd. Durham Plant.
※12	FMG	(Germany)	:	Fujitsu Mikroelektronik GmbH.
※13	FMI	(Gresham)	:	Fujitsu Microelectronics, Inc. Gresham Plant.
※14	FDI		:	Fujitsu Devices, Inc

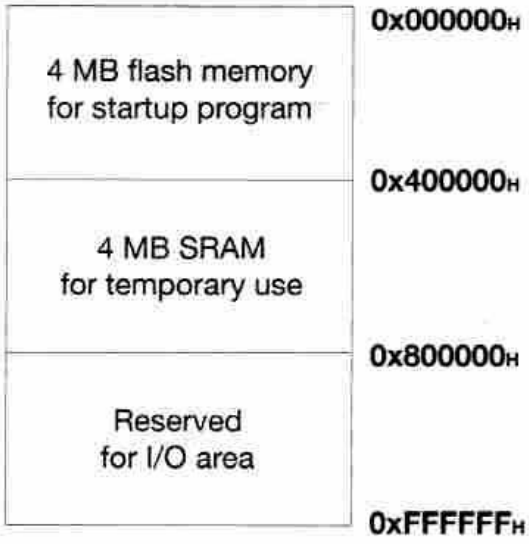
Flash Memory Application Note

CHAPTER 4. Application Note

■ **Contents** **page**

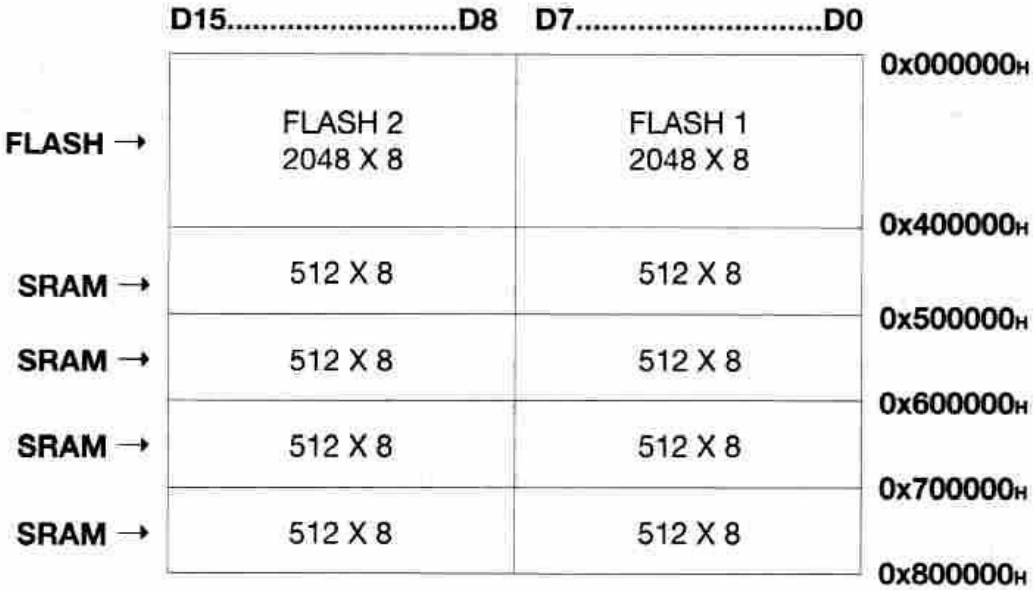
Flash Memory Application Note

A memory map is shown below.



The memory map above is logical and does not correspond to the physical placement of an actual device. This is because the 68000 MPU data bus is 16 bit, whereas the width of memory map above is 8 bit.

The memory map below shows the physical placement.



The device and placement address is decided in this way.

FUJITSU

FLASH MEMORY

DS05-20818-1E

PRELIMINARY

CMOS

2M (256K × 8)

MBM29F002T/002B/002ST/002SB

■ DISTINCTIVE CHARACTERISTICS

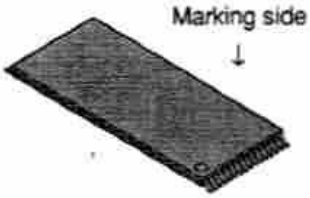
- **Single 5.0 V read, write, and erase**
  Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  Uses same software commands as E²PROMs
- **Package option**
  32-pin TSOP (Package suffix: PFTN-Normal Bend Type, PFTR-Reversed Bend Type) ... MBM29F002T/002B
- 32-pin PLCC ... MBM29F002T/002B
  40-pin TSOP (Package suffix: PTN-Normal Bend Type, PTR-Reversed Bend Type) ... MBM29F002ST/002SB
- **Minimum 100,000 write/erase cycles**
- **High Performance**
  90 ns maximum access time
- **Sector erase architecture**
  One 16K byte, two 8K bytes, one 32K byte, and three 64K bytes.
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Boot Code Sector Architecture**
  T=Top sector
  B=Bottom sector
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically write and verifies data at specified address
- **Data Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Low power consumption**
  20 mA typical active read current for Byte Mode
  28 mA typical active read current for Word Mode
  30 mA typical write/erase current
  25 uA typical standby current
- **Low Vcc write inhibit ≤ 3.2 V**
- **Sector protection**
  Hardware method disables any combination of sectors from write or erase operations
- **Temporary sector unprotection**
  Hardware method temporarily enables any combination of sectors from write or erase operations
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read in another sector within the same device

Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

5

MBM29F002T/002B/002ST/002SB

■ PACKAGE



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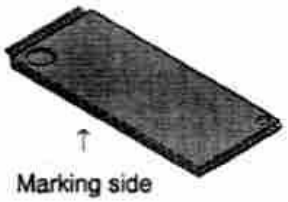

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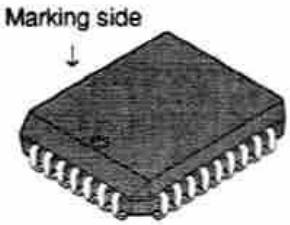
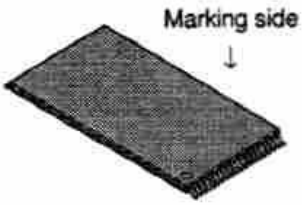
32-pin TSOP



(LCC-32P-M02)
32-pin PLCC



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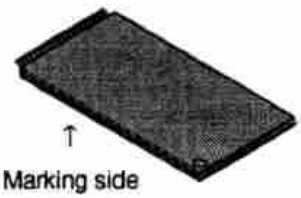

(FPT-40P-M07)

40-pin TSOP