The PCIe40 card

A large bandwidth acquisition module for High Energy Physics experiments.

High-energy physics studies the laws that regulate the universe at subatomicscale. For that purpose, subatomic paraticles are accelerated and brought to collision at high energies, today reaching tens of TeV.
The collisions occur in advanced machines at tens of MHz rates. Energy is reconverted into matter and new particles, unseen under ordinary conditions are created. To capture and study matter at this energy density, experiments are constructed around the interaction points of the colliders.

Figure 1: Large Hadron Accelerator

The Large Haddron Collider (LHC) at CERN is a gigantic ring accelerator of **27 km circonference** located on the Swiss France border close to Geneva. Particles are smashed together at 40 Millions collisions per seconds. Experiments located around 4 main interations points monitor the behaviour of already known particles and try to detect new ones that would be the proof of still unexplored physics phenomena. These main interaction points are called **LHCb** (study of the asymetry between matter and anti-matter), **ATLAS** and **CMS** (discovery of new particles) and **ALICE** (Simulation of the early conditions after the big bang).

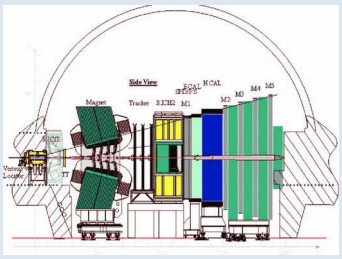
Figure 2: The LHCb detector

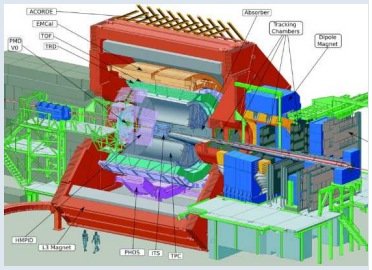
Figure 3: The ALICE detector

These experiments produce **hundreds of Terabytes** of information per second that would saturate any existing storage system in a couple of secconds. To avoid this, information is compressed and filtered in real time by sophisticated hardware systems before being sent to farms of thousands of computers running in parallel order to reduce drastically the data flow while keeping the most relevant interactions. Less than 0.01 % of data are finally stored for further study and analysis by researchers all around the world.

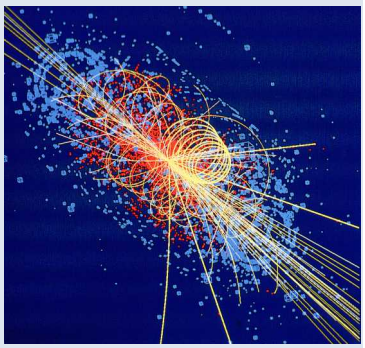
Figure 4: Collision results

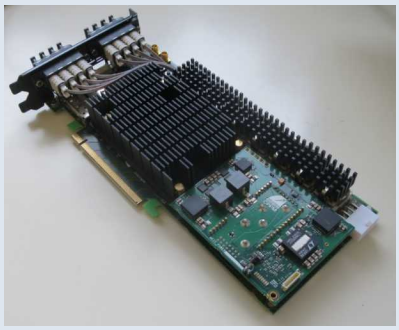
Figure 5: The PCIe40 card

The PCIe40 card, designed by the **Centre de Physique des Particules de Marseille** (CPPM), is a key element located at the frontier between physical detectors and the computer farm. Its role is to collect the event fragments which are the information produced by a subset of the different sensors, to assemble all those belonging to a same collision and to route them towards a single computer that will be able to process elaborated algorithmes for keeping or rejecting this event.

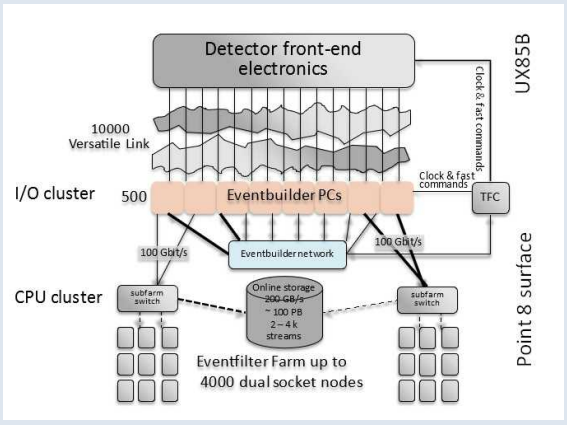

Figure 6: LHCb readout system

The readout system of LHCb is made of 500 PCIe40 cards collecting more than **30 Tbits of data per second** over 10000 optical links. Information collected is dspatched to a farm of 4000 computers for achieving the final filtering.
The card is used alsod by the ALICE experiment with a similar architecture.
The PCIe40 card contains **one of the largest FPGAs** currently available (Arria 10AX115S3F45E2SG from Intel) with more than **1.1 Million logic cells** for processing events in real time.
The connectivity with external world is made with 50 bidirectional high speed optical interfaces running at up to 10 Gbits/s each. The overall I/O bandwidth is up to **500 Gbits/s** in each direction. It is interfaced to the CPU by a **100 Gbits/s** PCIe Gen 3 interface. The card embedds very accurate PLLs allowing filter clocks with a total jitter of **less than 1 ps**.

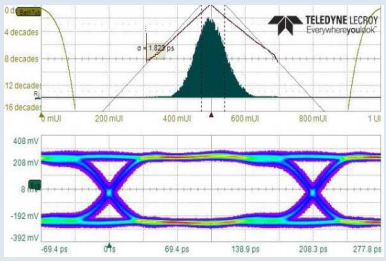

Figure 7: Optical links measurements

The design and manufacturing of such a card is a technological challenge requiring skills in many domains. The FPGA core consumes more than 50 A. Impedances have to be perfetly controlled to garanty the signal integrity of high speed signals.
The selection of the company able to build it has been a long process and a call for tender has been made in all countries of Europe. The chosen companies (**Somacis** for PCB and **FEDD** for assembly) have been short-listed for their expertise in high range technological products and their excellence in term of quality assurance, in particular for compliance to **IPC standards**.

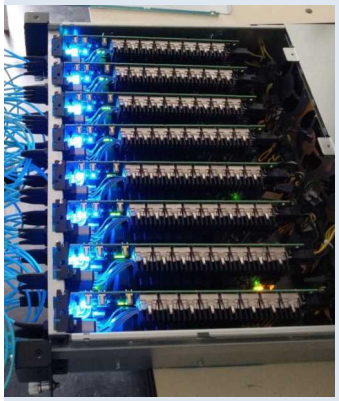
Figure 8: PCIe40 test bench

The production is fully automatized. After soldering, the card is stressed with several thermal cycles. Then a flying probes control checks the quality of connections. The card is fully tested with a functional test made by the assembly company.
When delivered at CERN an endurance test of 48 is run to detect early failures due to infant mortality.

More than 1250 PCIe40 have been produced

Contact information :
FEDD :
CPPM : Jean-Pierre Cachemiche – Tel +33-491 82 72 38 – Email : cachemi@cppm.in2p3.fr