PRÉSERVER
SAUVEGARDER
VALORISER

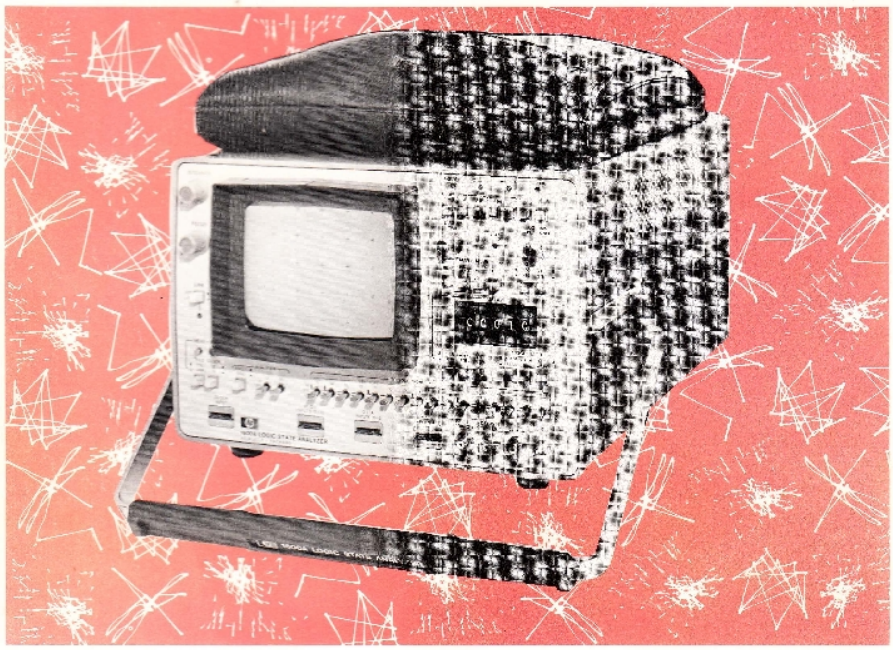
MODE D'EMPLOI ET DOCUMENTATION DE L'ANALYSEUR LOGIQUE HP 1600A

FICHE N° 3937

Période de fabrication : 1975-1999
Fabricant : fabricant non renseigné
Domaines : Informatique et Communication, Physique
Sous-domaines : Electronique
Organisme : Université de Rennes
Ville : Rennes
Modèle : HP 1600A
Matériaux : Papier

Description
Le mode d'emploi de l'analyseur logique Hewlett-Packard HP 1600 A était fourni avec l'appareil et conservé dans une trousse en cuir fixée au-dessus de l'instrument. D'une centaine de pages, il décrit les opérations possibles, l'ensemble des circuits et des fonctions qui le caractérisent (block diagrammes, circuits électroniques).

Utilisation
Cet analyseur d'état logique était utilisé par les enseignants des travaux pratiques d'électronique de la faculté des sciences de Rennes pour initier les étudiants aux circuits logiques et aux microprocesseurs. Le HP 1600A a été vendu à partir de 1975,



1600A

LOGIC STATE ANALYZER

OPERATING AND SERVICE MANUAL

HEWLETT hp PACKARD

COLORADO SPRINGS DIVISION

HP 1600A

Fig. 3. *Models 1600A and 1607A Logic State Analyzers work together to monitor and display 32-bit words, or work with independent clocks to examine the interaction between two digital machines. The combination of the two instruments is known as the Model 1608S. Model 1607A has most of the capabilities of Model 1600A and can work by itself using an oscilloscope or CRT monitor for the display.*

The two qualifier inputs may also be used with the trigger word, in effect giving an 18-bit trigger word.

Data may be clocked in at rates up to 20 MHz. This speed allows tests to be conducted at the full operating rate of most digital systems, thereby uncovering faults caused by circuit response—faults that do not occur when a system is tested by single-stepping it at a slow rate.

Positioning of the trigger word on the display has been made more flexible in the new instrument. As before, in the START DISPLAY mode, the trigger word appears at the top of the displayed table and the next fifteen words follow below. In the END DISPLAY mode, the trigger word appears at the bottom with the previous fifteen words above. In either case, the trigger word is brightened to show its position. Now the digital delay may be used with the END DISPLAY as well as the START DELAY mode, making it possible to display events both prior to and immediately following the trigger word. The word at the top of the display is the word that occurs fifteen clock periods before the trigger word minus the selected delay. If the delay is less than fifteen, the trigger word appears brightened part way down the display.

Another added display mode is known as partial display. This occurs automatically whenever the rate of the clocks qualified by the DISPLAY qualifiers is below 60 Hz. If the instrument is in the START DISPLAY mode, the display shows the trigger word as soon as it occurs (or the first word following the selected delay) and fills in each successive word as it is clocked in. Previously the user had to wait for sixteen words to accumulate before the display would show what had occurred.

In the case of partial display in the END DISPLAY mode, each word is entered at the bottom of the display, pushing the others up. When the display is full, each new word entering at the bottom pushes the top word off the display. This continues until trigger conditions are met.

An "arm" mode is now provided for the trigger. In this mode, the instrument does not respond to the trigger word unless armed by a pulse at its ARM input. This prevents the data acquisition cycle from being initiated until some other event occurs.

Dual Data

Model 1600A has an auxiliary memory for storage of data. A front-panel pushbutton (STORE A → B) transfers the data stored in the main memory (A) to the auxiliary memory (B). The contents of each memory may be displayed separately or both may be displayed side by side for comparisons.

To make it easier to compare stored data with new data, a comparison mode [A & (A⊕B)] may be selected. The contents of the A memory are then displayed on the left half of the display while the right half shows how the contents of B differ from A—bit positions where the two memories are identical are displayed as 0's, and bit positions where they differ are displayed as 1's (Fig. 4). In addition, the 1's are brightened to make them easier to identify.

To help find elusive errors, the instrument may be operated in a HALT A≠B mode in which the A memory acquires the data in repeating data acquisition cycles until there is a difference between the contents of memories A and B. The instrument then reverts to the single-cycle mode and stops acquiring data when the current cycle is completed.

Map Display

A more comprehensive view of the operation of digital machines is provided by a new capability in Model 1600A. This is the MAP mode.

When operating in the MAP mode, the new logic state analyzer presents a digital word simply as a dot on the CRT display. The position of the dot is determined by the word, one half of the word giving the x-axis position and the other half giving the y-axis po-

Fig. 1. *Model 1600A Logic State Analyzer monitors digital data appearing on as many as 16 lines and displays the data as words of 1's and 0's in tabular form running from top to bottom on the left half of the display. The right half of the display is used for data stored in an auxiliary memory or for data acquired by a companion instrument, the Model 1607A.*

is pressed, initiating a new data acquisition cycle.

The trigger may be any of the words in the data stream. A front-panel switch register enables the user to select the word that serves as the trigger. It is thus possible to view any part of an executing digital program by using the first word of the sequence as a trigger. The delay capability may be used to page through long sequences. Or, the digital sequence leading up to an unallowed state caused by a fault may be examined, using the unallowed word as the trigger.

The trigger word also causes the instrument to generate an output pulse that can serve as a trigger for an oscilloscope or other instruments in a test setup. This makes it possible to view the waveforms that occur at a defined point in time with respect to the trigger word.

To provide flexibility in applications of the instrument, data may be clocked in on either the positive-going or negative-going edge of the clock pulses, the data may be interpreted as either positive-true or negative-true logic, and the logic threshold is adjustable. The miniature probe system developed for the Model 1601L, which facilitates making the many closely-spaced connections to the circuit under test, is also used with the new logic state analyzer (Fig. 2).

Branching Out

The new Model 1600A Logic State Analyzer broadens this basic capability by being able to look at 16 lines simultaneously, four more than the 12-bit capability of the earlier Model 1601L. When working with Model 1607A, Model 1600A can look at and display data appearing at 32 points (Fig. 3).

Two qualifier inputs have been added. When used in the QUALIFIER DISPLAY mode, these make it possible to be selective in clocking data into memory. For example, when monitoring a multi-use bus that has time-multiplexed addresses, instructions, and data, only the information pertinent to a particular operation need be stored for display.

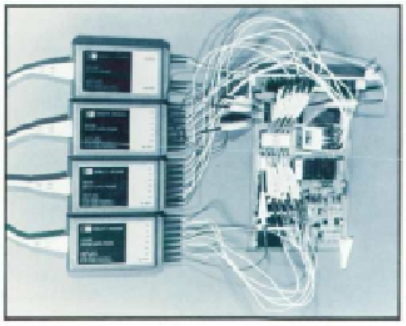


Fig. 2. *Miniature probes facilitate connections to closely-spaced test points. The probes are connected through short leads to input circuits within the pods to minimize circuit loading.*

The Logic State Analyzer, a Viewing Port for the Data Domain

A new logic state analyzer has expanded capabilities that speed the location of the sources of problems in digital systems and broaden the range of problems that can be resolved with this class of instrument.

by Charles T. Small and Justin S. Morrill, Jr.

ENGINEERS DEVELOPING DIGITAL systems—especially those that involve microprocessors—now find themselves more concerned with word flow than with waveforms. But until recently, it was considerably more difficult to perceive word flow within an operating system than it was to view waveforms.

This situation was improved two years ago when a new kind of instrument, the parallel-mode logic state analyzer, was introduced.[1] The first of these instruments, the Hewlett-Packard Model 1601L, monitored data buses or other multinodal locations in a digital system, "captured" a sequence of digital words as it occurred there, and displayed the sequence as a table of 1's and 0's.

With the insight provided by this instrument, it became much easier to trace data flow and track down problems in digital systems. Digital designers who have had the opportunity to use this instrument now find it indispensable for analyzing and troubleshooting the digital systems on which they are working.

New Directions

Two years' experience with the Model 1601L has uncovered a number of additional capabilities that such an instrument might have. These capabilities have now been incorporated in a new logic state analyzer, Model 1600A, which works with or without a companion instrument, Model 1607A.

Basically, the Model 1600A (Fig. 1) works like the earlier Model 1601L: digital data appearing in parallel on several different lines is monitored through a multi-probe system and clocked into the instrument in synchronism with the clock or other pulses from the system under test. When a preselected trigger word appears on the data lines, the instrument stores the trigger word and the next 15 words and then displays the stored data in tabular form. Digital delay may be introduced making it possible to view the 16 words that occur as many as 99,999 clock periods after the trigger. Alternatively, the instrument may be set to store data continuously and then stop acquiring data when the trigger occurs. The 15 words leading up to the trigger word are thus captured for study.

Data acquisition and display cycles may alternate repetitively, or data may be acquired once and then displayed continuously until the RESET pushbutton

Cover: *Multichannel is the byword as new test instruments are developed in response to the accelerating rush to digital electronics. Described in this issue is the latest logic state analyzer, which gives a multiport view of what's happening in an operating digital system, and an eight-channel word generator for supplying the multichannel bit patterns needed for digital testing.*

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