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LIVRE : RANDOM TESTING OF DIGITAL CIRCUITS

FICHE N° 9943

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Fabricant : fabricant non renseigné
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Description

Titre traduit : Tests aléatoires de circuits intégrés

"Random testing of digital circuits" est un livre broché de 475 pages, daté de 1998, rédigé en anglais mais édité par le LAG, dont le titre traduit pourrait être "test de circuits digitaux selon des méthodes aléatoires"

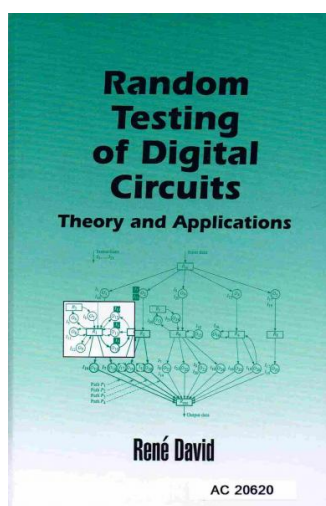
Son auteur est René David, un enseignant/chercheur de l'IMAG de Grenoble. Il a travaillé dès les débuts au LAG, le Laboratoire d'Automatique de Grenoble, sous la direction de René Perret.

L'usage de la langue anglaise répond à l'objectif de diffusion au niveau international. Le fait que l'auteur soit français et grenoblois montre le rayonnement de Grenoble dans le domaine de l'informatique et des automatismes.

Le livre comprend de nombreux schémas et tableaux explicatifs des méthodes mises en œuvre.

Utilisation

Les méthodes aléatoires de test répondent à des problématiques de test portant sur des circuits digitaux qui deviennent de plus en plus complexes au fil du temps. Pour éviter que cette complexité croissante ne conduise à des temps de tests de plus en plus longs, la méthode aléatoire vise à s'assurer que chaque élément du circuit complexe soit testé au moins une fois, mais pas dans toutes les configurations possibles, ce qui permet de limiter au minimum les temps d'exécution des tests.



Because of the difficulty of generating test sequences for large circuits, design methods aiming at reducing this difficulty have been developed; these generally consist in changing the circuit (DFT). An important DFT method, the scan design, is presented in the next section.

1.1.2 Scan design

Full scan design is a technique of design for testability whose aim is to transform a sequential circuit in order to test it like a combinational circuit. In general, scan design consists in adding a number of scan flip-flops to the circuit. The principle is illustrated in Figure 1.2. Then, we return to the principle.

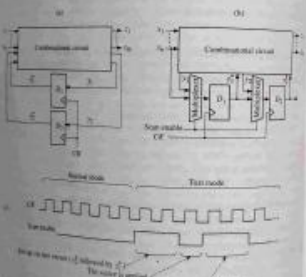


Figure 1.2: Diagram of scan design. (a) A sequential circuit. (b) Multiplexer circuit with a scan flip-flop. (c) A scan flip-flop.

Figure 1.2 illustrates the principle of scan design. (a) A sequential circuit. (b) Multiplexer circuit with a scan flip-flop. (c) A scan flip-flop.

Figure 1.2a represents an n -input, m -output, 2-internal variable, sequential circuit. It is made up of an $(n + 2)$ -input, $(m + 2)$ -output, combinational circuit, and of two D flip-flops. The internal state (the output y , at time t) becomes the input y_t at time $t + 1$. Figure 1.2b represents the same circuit where a multiplexer provides each D flip-flop. The multiplexer is controlled by the Boolean variable *scan enable*; when *scan enable* = 0, the variable y_t is the input of the flip-flop D; when *scan enable* = 1, the flip-flops are connected as a shift register (scan path), whose input is x_t .

Figure 1.2c illustrates the behavior of the circuit in Figure 1.2b. In normal mode, *scan enable* remains 0 and the circuit behaves as in Figure 1.2a. In test mode, the behavior is as follows: 1) When the variable *scan enable* = 1, during a series of s clock pulses (if s is the number of internal variables, $s = 2$ in our example), the values required in the flip-flops are set up by shifting from the input x_t (the required y_t^0 followed by the required y_t^1). 2) Then *scan enable* = 0 for one clock pulse and the desired $(n + 2)$ -input test vector is applied; it is made up of the Boolean variables present on $x_t, \dots, y_t$, and the s outputs of the flip-flops. 3) The outputs $z_1, \dots, z_m$ can immediately be observed, and a series of s clock pulses when *scan enable* = 1, shifts the s other outputs, stored in the flip-flops, to the output of the scan flip-flop. During this series of s pulses, the next vector of values required in the flip-flops is set up. And so on.



Figure 1.3: Boundary Scan.

In the sequel, we will explicitly distinguish between the interior of a circuit and the exterior of a circuit. Basically, we will consider that a circuit (i.e., all interior parts) corresponds to a chip; however, it could be a board or a subsystem. As illustrated in Figure 1.3, boundary scan allows the circuit to be

Section 1.1.2, Figure 1.2.

scan flip-flops adjacent to and often physically adjacent to the input/output pins of the chip. The sequence in Figure 1.3 allows the circuit to function normally; all the registers are used without any shifting. It also allows the normal logic to be tested; input data are applied from the input register and the normal output of the circuit, and the corresponding responses are latched in the normal register; the results in the internal register can be shifted out, and verified. Scan design (including boundary scan) is useful because it allows good observability and good controllability of the internal memory elements of the circuit. In addition, test pattern generation is simplified, since it is performed on a combinational circuit (in case of full scan). However, scan design does not give a satisfactory answer to all test problems, as is explained in the following section.

1.1.3 Some fundamental difficulties leading to BIST

The testing of large and complex integrated circuits presents some fundamental difficulties which naturally lead to the idea of built-in self-test, i.e., a design including some test device on the chip. A BIST may be used with or without scan design.

1) If the circuit under test and the external tester are based on the same technology, a universal test sequence cannot be applied at the external level of the circuit; the tester is slower than the tested circuit (hence some delay problems arise only at high speed cannot be detected). On the other hand, if a test sequence is hardwired on the chip itself, it may be applied at the external level of the circuit.

2) Scan design improves controllability and observability. However, it has some disadvantages when it is built in the circuit, since an input vector is set by shifting its components, the necessary time between two successive vectors cannot correspond to the nominal speed, and the test time is long.

3) The internal complexity increases more quickly than the number of possible paths (for example that we are able to produce (with a reasonable number of paths) whose size dimension is d). The number of components increases proportionally to the surface; hence, the number increases proportionally to d^2 . In addition, each component increases smaller from year to year. Hence the number of components is still greater; on the other hand the test sequence is becoming more difficult to test a circuit from the limited number of pins. If the test sequence generator and the test evaluator are built in the chip, controllability and observability may be improved by additional inputs and outputs to the internal circuit, respectively, without using extra pins (over the available pins).

4) If the chip has a large number of pins, its surface must be small.

corresponding wires come from the sequence generator or go to the test evaluator.

An advantage of BIST is that the test device is the same throughout the circuit life. There is no need to use the same test device in a field test; the same test device is used both by the manufacturer and the user.

Other advantages (particularly avoidance of test pattern generation, often cited in the literature) derive from the fact that pseudorandom tests are used in BIST. They will be explained at the end of Section 1.2.

1.2 BUILT-IN SELF-TEST

Various routines have been used over twenty years for the ability of a circuit to test itself. Today, the name *built-in self-test* (BIST), merging built-in test (BIT) with self-test, is widely used. Two main categories may be considered: on-line BIST and off-line BIST.

1.2.1 On-line BIST

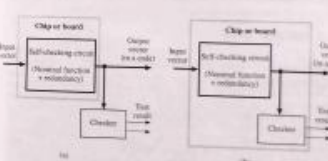


Figure 1.4: On-line BIST. (a) The checker is not in the circuit. (b) The checker is in the circuit.

Figure 1.4 illustrates on-line BIST. The circuit is self-checking; informally, the circuit implements the nominal function (i.e., the basic function that the circuit is expected to perform) but also contains a redundant part in order to verify the correct behavior. The output vector is encoded, for example by a

Pour nous citer :

Base de la Mission nationale de sauvegarde et de valorisation du patrimoine scientifique et technique contemporain, PATSTEC, Livre : Random testing of digital circuits (fabricant non renseigné), <https://www.patstec.fr/ressources/objets/detail?id=27674>, consulté le 2026-07-26